AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

a sample circuit configured to (i) detect a state of an input signal and (ii) present a plurality of intermediate signals each representative of said state of said input signal during a plurality of clock cycles; and

a selection circuit configured to present a filtered signal in response to (i) a selected number of said intermediate signals having a lost state and (ii) a multi-bit selection signal representing a filtering value, wherein said filtered signal indicates said input signal has been lost when said selected number of lost states is greater than said filtering value.

2. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said sample circuit comprises:

a detect circuit configured to (i) detect said state of said input signal and (ii) present a detected signal representing said state of said input signal; and

a plurality of shift registers configured to (i) sample said detected signal in each of said clock cycles and (ii) present said intermediate signals in parallel.

3. (PREVIOUSLY PRESENTED) The apparatus according to claim 2, wherein said sample circuit further comprises a second shift register circuit configured to synchronize said detected signal to a clock signal defining said clock cycles.

4. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said selection circuit comprises:

a plurality of logic gates each configured to present a second intermediate signal in response to at least two of said intermediate signals; and

a multiplexer configure to multiplex said second intermediate signals to present said filtered signal as determined by said multi-bit selection signal.

5. (PREVIOUS PRESENTED) The apparatus according to claim 4, wherein each of said logic gates is configured to (i) receive one of said intermediate signals and one of said second intermediate signals and (ii) present another one of said second intermediate signals.

6. (CURRENTLY AMENDED) The apparatus according to claim 1, further comprising a second selection circuit configured to present a second filtered signal in response to a second selected number of said intermediate signals having a second predetermined

state, said second selected number defined by a second multi-bit selection signal.

7. (CURRENTLY AMENDED) The apparatus according to claim 6, further comprising a status circuit configured to present a status signal indicating one of (i) a signal lost and (ii) a signal present to in response to both said filtered signal and said second filtered signal.

8. (ORIGINAL) The apparatus according to claim 7, wherein said selected number and said second selected number are programmable.

9. (PREVIOUSLY PRESENTED) The apparatus according to claim 8, wherein said selected number has a value different than said second selected number.

10. (PREVIOUSLY PRESENTED) The apparatus according to claim 9, wherein said predetermined state comprises a loss-of-signal state and said second predetermined state comprises a signal present state.

11. (CURRENTLY AMENDED) A method of filtering an input signal, the method comprising the steps of:

(A) detecting a state of said input signal;

(B) presenting a plurality of intermediate signals in parallel, each of said intermediate signals representing said state of said input signal during a plurality of clock cycles; and

(C) presenting a filtered signal in response to (i) a selected number of said intermediate signals having a lost state and (ii) a multi-bit selection signal representing a filtering value, wherein said filtered signal indicates said input signal has been lost when said selected number lost states is greater than said filtering value.

12. (ORIGINAL) The method according to claim 11, further comprising the steps of:

presenting a detected signal representative of said state of said input signal in response to detecting; and

sampling said detected signal in each of said clock cycles to present said intermediate signals.

13. (ORIGINAL) The method according to claim 12, further comprising the step of synchronizing said detected signal to a clock signal defining said clock cycles in response to detecting.

14. (CURRENTLY AMENDED) The method according to claim 11, wherein step C comprises the sub-steps of:

presenting a plurality of signals each in response to at least two of said intermediate signals; and

multiplexing said signals to present said filtered signal as determined by said multi-bit selection signal.

15. (ORIGINAL) The method according to claim 14, wherein presenting said signals comprises the sub-step of performing a plurality of logical operations each receiving one of said intermediate signals and a one of said signals to present one of said signals.

16. (CURRENTLY AMENDED) The method according to claim 11, further comprising the step of presenting a second filtered signal in response to a second selected number of said intermediate signals having a second predetermined state, said second selected number defined by a second multi-bit selection signal.

17. (CURRENTLY AMENDED) The method according to claim 16, further comprising the step of presenting a status signal indicating one of (i) a signal lost and (ii) a signal present responsive to both said filtered signal and said second filtered signal.

18. (ORIGINAL) The method according to claim 17, further comprising the step of programming said selected number and said second selected number.

19. (PREVIOUSLY PRESENTED) The method according to claim 18, wherein said selected number has a value different than said second selected number.

20. (CURRENTLY AMENDED) A circuit comprising:

means for detecting a state of an input signal, said state consisting one at a time of (i) a loss-of-signal state and (ii) a signal present state;

means for presenting a plurality of intermediate signals each representing said state of said input signal during a plurality of clock cycles; and

means for presenting a filtered signal in response to (i) a selected number of said intermediate signals having a lost state and (ii) a multi-bit selection signal representing a filtering value, wherein said filtered signal indicates said input signal has been lost when said selected number lost states is greater than said filtering value.